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1 C-configurability and built-in-test of reconfigurable processor array interconnection networks

Henling, B.; Soma, M.;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Vol 39 , Issue: 5 , May 1992

Pages:302 - 311

[\[Abstract\]](#) [\[PDF Full-Text \(772 KB\)\]](#) IEEE JNL

2 A Convex Programming Approach for Generating Guaranteed Passive Approximations to Tabulated Frequency-Data

Coelho, C.P.; Phillips, J.; Silveira, L.M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 2 , Feb. 2004

Pages:293 - 301

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) IEEE JNL

3 High-level language abstraction for reconfigurable computing

Najjar, W.A.; Bohm, W.; Draper, B.A.; Hammes, J.; Rinker, R.; Beveridge, J.; Chawathe, M.; Ross, C.;

Computer , Volume: 36 , Issue: 8 , Aug. 2003

Pages:63 - 69

[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) IEEE JNL

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1 A novel and efficient routing architecture for multi-FPGA systems

Khalid, M.A.S.; Rose, J.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 8 , Issue: 1 , Feb. 2000

Pages:30 - 39

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) IEEE JNL

2 A memory-controlled crosspoint switch using E-beam restructuring

Fried, J.; Daly, E.; Lyszczarz, T.; Copperman, M.;

Solid-State Circuits, IEEE Journal of , Volume: 24 , Issue: 1 , Feb. 1989

Pages:183 - 187

[\[Abstract\]](#) [\[PDF Full-Text \(828 KB\)\]](#) IEEE JNL

3 MEMS-based capacitor arrays for programmable interconnect and R applications

Duewer, B.E.; Wilson, J.M.; Winick, D.A.; Franzon, P.D.;

Advanced Research in VLSI, 1999. Proceedings. 20th Anniversary Conference on , 21-24 March 1999

Pages:369 - 377

[\[Abstract\]](#) [\[PDF Full-Text \(96 KB\)\]](#) IEEE CNF

4 Annealed embeddings of communication patterns in an interconnect cached network

Gupta, V.; Schenfeld, E.;

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1 Fault-tolerant content addressable memory

Lo, J.-C.;

Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceedings., 1993 IEEE International Conference on , 3-6 Oct. 1993
Pages:193 - 196

[\[Abstract\]](#) [\[PDF Full-Text \(332 KB\)\]](#) **IEEE CNF**

2 Methodologies for testing embedded content addressable memories

Mazumder, P.; Patel, J.H.; Fuchs, W.K.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 7 , Issue: 1 , Jan. 1988
Pages:11 - 20

[\[Abstract\]](#) [\[PDF Full-Text \(852 KB\)\]](#) **IEEE JNL**

3 On fault modeling and testing of content-addressable memories

Al-Assadi, W.K.; Jayasumana, A.P.; Malaiya, Y.K.;

Memory Technology, Design and Testing, 1994., Records of the IEEE International Workshop on , 8-9 Aug. 1994
Pages:78 - 83

[\[Abstract\]](#) [\[PDF Full-Text \(428 KB\)\]](#) **IEEE CNF**

4 Linear time fault simulation algorithm using a content addressable memory

Ishiura, N.; Yajima, S.;